UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,590	03/19/2004	Larry E. Hand	D2A1250-1	9253

42671 7590 10/30/2008

LAW OFFICES OF MARK L. BERRIER
3811 BEE CAVES ROAD
SUITE 204
AUSTIN, TX 78746

EXAMINER	
SELLERS, DANIEL R	

ART UNIT	PAPER NUMBER
2614	

MAIL DATE	DELIVERY MODE
10/30/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/805,590	HAND ET AL.	
	Examiner	Art Unit	
	DANIEL R. SELLERS	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 8-16* is/are rejected.

7)☒ Claim(s) *5-7 and 17-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-19 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. **Claims 1-4, 8, and 10-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasuda (previously cited) further in view of Cory (previously cited) and Reilly, US 5,390,180 A.

4. Regarding **claim 1**, Yasuda teaches a multi-channel audio amplifier system (¶ 0011) comprising:

a plurality of audio amplifier channels (¶ 0025 and ¶ 0027), *wherein each channel includes a sample rate converter* (¶ 0026, figure 1, units 110, 120, and 130, and figure 2) *configured to*

receive samples of an input audio data stream (¶ 0028 and figure 1, unit 1), *store the samples in an input buffer, retrieve samples from the input buffer* (¶ 0036-0037 and figure 2, unit 13), *and*

convert the samples to a re-sampled audio data stream (¶ 0039 and figure 2, unit 21) , *and*

a buffer management unit coupled to the input buffer (¶ 0041 and figure 2, unit 25) *and configured to maintain*

a write pointer indicating a position in the input buffer to which a next sample will be written (¶ 0041) *and*

a read pointer indicating a position in the input buffer from which a next sample will be read (¶ 0041),

wherein the buffer management unit is configured to determine an actual difference between the values of the read and write pointers (¶ 0043),

wherein the buffer management unit is further configured to control a rate at which samples are read from the input buffer to achieve a target difference between the values of the read and write pointers (¶ 0049);

wherein for a first one of the channels, the target difference comprises a predetermined value; wherein for the remainder of the channels, the target difference comprises the actual difference between the values of the read and write pointers of the first one of the channels; and

wherein the buffer management unit is configured to read samples from the input buffer in an order in which the samples were written to the input buffer without skipping or re-reading any of the samples stored in the input buffer.

Yasuda teaches a PWM, or class-D, amplifier for use in a multi-channel system, wherein a controller directs the read and write pointers in several channels (see figure 1, units 101, 110, 120, and 130). Yasuda however does not disclose the features of a target difference for a first of the several channels, and an actual difference equal to the target difference for the remainder of the channels.

Cory teaches a method for synchronizing plural channels in an elastic buffer, or FIFO memory (column 1, lines 12-52, column 2, line 62 - column 3, line 16, and column 4, line 20 - column 5, line 14). Cory does not teach audio data, however it would have been obvious at the time of the invention for one of ordinary skill in the art to contemplate the usefulness of this FIFO buffer control, because Yasuda also teaches FIFO buffers, or ring buffers. Specifically, Cory teaches controlling the read pointer to achieve a target difference for a first one of the channels (column 19, lines 7-23), controlling the read pointers of the slave buffers based on the actual difference in the master buffer (column 29, lines 56-66). It would have been obvious for one of ordinary skill in the art at the time of the invention to combine the teachings of Yasuda and Cory for the purpose of synchronizing the plural channels and reducing misalignment of the audio data. Therefore, the combination teaches a method of controlling the synchronization between multiple buffers using a master and slave setup, but the

combination does not appear to be configured to not skip or re-read samples while synchronization is performed.

Reilly teaches a buffer, wherein the rate of outgoing read data is tied to the rate of incoming written data in a synchronous optical network (abstract). Specifically, Reilly teaches a buffer, with a fullness indicator, which receives data at one synchronized rate and outputting the data at a desynchronized rate (e.g. desynchronized to the reception rate) (see column 5, lines 1-18). Reilly teaches the "desynchronized clock" is derived from a phase accumulator (see column 7, line 50 - column 8, line 5, figure 3, units 1, 3, 7, 9, 10, and 12, and figure 5, units 7 and 71b). It would have been obvious for one of ordinary skill in the art at the time of the invention to combine the teachings of Yasuda, Cory, and Reilly for the purpose of providing a better quality audio output. It would have been obvious that better quality audio can be provided by reading out all the samples without skipping or replaying samples while providing synchronization for multiple audio outputs in a network.

5. Regarding **claim 2**, the combination teaches the system of claim 1, further comprising these features. It is implicit there is an interconnect to convey the actual difference between the first channel and the remainder channels as taught by the master-slave method by Cory.

6. Regarding **claim 3**, the combination teaches the system of claim 1, further comprising these features (see Reilly, column 7, line 50 - column 8, line 5, figure 3, units 1, 3, 7, 9, 10, and 12, and figure 5, units 7 and 71b).

7. Regarding **claim 4**, the combination teaches the system of claim 3, further comprising these features (see Reilly, column 8, lines 6-15 and figure 5, units 71b, 72, 73, and 74).

8. Regarding **claim 8**, see the preceding argument with respect to claim 1. The combination of Yasuda, Cory, and Reilly teaches these features.

9. Regarding **claim 10**, see the preceding argument with respect to claim 1. The combination teaches the method of claim 8, wherein the method is implemented in a plurality of sample rate controllers.

10. Regarding **claim 11**, see the preceding argument with respect to claim 1. The combination teaches the method of claim 10, wherein the buffers comprise input buffers of the sample rate controllers.

11. Regarding **claim 12**, see the preceding argument with respect to claim 1. The combination teaches the method of claim 10, wherein each sample rate controller is implemented in a channel of a multi-channel audio amplification system. Yasuda teaches each sample rate controller converts two channels, and illustrates in figure 1, three separate controllers for six channels of audio. It would have been obvious to separate each controller to handle one channel individually and double the components so that six controllers convert six channels.

12. Regarding **claim 13**, see the preceding argument with respect to claim 1. The combination teaches the method of claim 8, further comprising transmitting the difference between the read and write pointers of the first one of the buffers from a

buffer management unit in the first one of the buffers to buffer management units in the remainder of the buffers (see Cory, column 22, lines 25-40 and column 29, lines 56-66).

13. Regarding **claim 14**, see the preceding argument with respect to claim 1. The combination teaches a system comprising these features.

14. Regarding **claim 15**, see the preceding argument with respect to claim 3. The combination teaches these features.

15. Regarding **claim 16**, see the preceding argument with respect to claim 4. The combination teaches these features.

16. **Claim 9** is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Yasuda, Cory, and Reilly as applied to claim 8 above, and further in view of Cooke (previously cited).

17. Regarding **claim 9**, see the preceding argument with respect to claim 1. The combination teaches the method of claim 8, wherein the method is implemented in a multi-channel audio amplification system. The combination teaches these features, however does not explicitly state the convolution operation uses polyphase filter coefficients (Yasuda, ¶ 0067-0068).

In a related art, Cooke teaches the use of an input buffer in a sample rate conversion system (abstract and figure 4). Specifically, Cooke teaches the use of polyphase filter coefficients (column 5, line 58 - column 6, line 10). It would have been obvious for one of ordinary skill in the art at the time of the invention to combine the teachings of Yasuda, Cory, Reilly, and Cooke for the purpose of producing higher

quality audio. Cooke teaches the polyphase filter coefficients produce output data approximating signal characteristics of input data as if it had originally been sampled at the resampled rate (column 6, lines 1-3).

Allowable Subject Matter

18. **Claims 5-7 and 17-19** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

19. Regarding **claim 5**, see the preceding argument with respect to claim 4 under 35 USC 103, wherein the combination teaches the features of claim 4. However, the prior art does not appear to teach or reasonably suggest an error signal transmitted to the low pass filter to control a sample rate count.

20. Regarding **claims 6 and 7**, see the preceding argument with respect to claim 5. These claims depend from claim 5, wherein the prior art does not appear to teach or reasonably suggest the features of claim 5.

21. Regarding **claim 17**, see the preceding argument with respect to claim 5. The prior art does not appear to teach or reasonably suggest these features.

22. Regarding **claims 18 and 19**, see the preceding argument with respect to claim 17. These claims depend from claim 17, wherein the prior art does not appear to teach or reasonably suggest the features of claim 17.

Conclusion

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Curtis et al., US 6,389,139 B1 (previously cited) - teaches a network audio system using in a serial connection (see figure 7);

O'Brien, US 6,429,737 B1 (previously cited) - teaches a multi-channel audio amplifier using PWM amplification and utilizing a global system timing (abstract and figure 1, unit 123 and 124);

Midya, US 2003/0042976 A1 (previously cited) - teaches a PWM amplification system using sample rate converters (see figures 1 and 8); and

Stanley, US 6,683,494 B2 (previously cited) - teaches another PWM amplification system using a master-slave clock system (see figure 1, units 18 and 30, figure 4, units 18, and 232, and column 10, lines 51-60).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL R. SELLERS whose telephone number is (571)272-7528. The examiner can normally be reached on Monday to Friday, 9am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Curtis Kuntz can be reached on (571)272-7499. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Daniel R. Sellers/
Examiner, Art Unit 2614
/CURTIS KUNTZ/
Supervisory Patent Examiner, Art Unit 2614